(FILE 'USPAT' ENTERED AT 16:44:24 ON 12 SEP 1999)

L1	403105	S	PATTERN?
L2	61	S	PATTERNLESS
L3	61	S	L1 AND L2
L4	61	S	L1 (P) L2
L5	403023	S	PATTERN###
L6	29	S	L5 (P) L2
L7	1	S	L6 (P) SWITCH?
L8	0	S	L6 (P) ADDRESS?
L9	0	S	L4 (P) ADDRESS?
L10	515	S	BURST? (P) PIPELIN?
L11	167	S	L10 (P) MODE
L12	7	S	L11 (P) SWITCH?
L13	1	S	L6 (P) MODE
L14	2	S	L6 (P) MEMORY

US PAT NO: 5,652,724 [IMAGE AVAILABLE] L12: 4 of 7

SUMMARY:

BSUM(11)

An . . . standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed **burst mode** of operation is provided where multiple sequential accesses occur following a single column address, and data is input and output relative to the /CAS control signal. In the **burst mode** of operation the address is incremented internal to the device eliminating the need for external address lines to **switch** at high frequencies. Read /Write commands are issued once per **burst** access eliminating the need to toggle the Read /Write control line at high speeds. Only one control line per memory. . . each /CAS typically controls only a byte width of the data bus. A data output buffer has a two stage **pipeline mode** of operation which allows for further speed increases by latching read data in an intermediate data latch, and allowing internal. . . . the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to **switch** between a standard non-**burst mode** and a high speed **burst mode** allows the device to be used to replace standard devices, and eliminates the need to **switch** to more complex high speed memory devices. Internal address generation with a **pipelined** data output provides for faster data access times than is possible with either fast page **mode** or EDO DRAMs. This high speed operation eliminates the need to interleave memory devices in order to attain a high. . . from the memory. Operating frequencies significantly higher than 50 megahertz are possible with this architecture due to internal address generation, **pipelined** read circuitry, an extended valid data output period, and a single lightly loaded control signal operating at the operating frequency. . .

DETDESC:

DETD(11)

Programmability of the **burst** length, /CAS latency and address sequences may be accomplished through the use of a **mode** register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the **mode** register control the required circuits on the DRAM. **Burst** length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may. . . be provided. For a latency of 1, the intermediate data latch is bypassed. For a latency of 3, an additional **pipeline** stage may be added. It may be desirable to place this additional **pipeline** stage in the address path, or in the read data path between the memory array and the first intermediate data latch. Other **burst** length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The. . . programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The **burst** length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed **burst mode** only, selecting between standard fast page **mode** (non-EDO) and **burst mode**, and using the output enable pin (/OE) 42 in combination with /RAS to select between **modes** of operation. Also, a WCBR refresh cycle could be used to select the **mode** of operation rather than a control signal in combination with /RAS. A more complex memory device may provide

additional **modes** of operation such as **switching** between fast page **mode**, EDO page **mode**, static column **mode** and **burst** operation through the use of various combinations of /WE and /OE at /RAS falling time. One **mode** from a similar set of **modes** may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired **mode**. Alternately, a device with multiple **modes** of operation may have wire bond locations, or programmable fuses which may be used to program the **mode** of operation of the device.

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